Design, Operation and Flexible Control of a DSTATCOM Operating in Voltage Control Mode

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ABSTRACT: A distribution static compensator (DSTATCOM) is used for load voltage regulation and its performance mainly depends upon the feeder impedance and its nature (resistive, inductive, stiff, non-stiff). However, a study for analyzing voltage regulation performance of DSTATCOM depending upon network parameters is not well defined. This paper aims to provide a comprehensive study of design, operation, and flexible control of a DSTATCOM operating in voltage control mode. A detailed analysis of the voltage regulation capability of DSTATCOM under various feeder impedances is presented. Then, a benchmark design procedure to compute the value of external inductor is presented. A dynamic reference load voltage generation scheme is also developed which allows DSTATCOM to compensate load reactive power during normal operation, in addition to providing voltage support during disturbances. Simulation and experimental results validate the effectiveness of the proposed scheme.

KEYWORDS: DSTATCOM, Voltage regulation, load voltage generation, voltage control mode

I.INTRODUCTION

The voltage regulation performance of DSTATCOM mainly depends upon the feeder impedance and its nature (resistive, inductive, stiff, non-stiff). For voltage control mode (VCM) operation of DSTATCOM and/or grid connected inverters, the idea of inserting an external inductor in line has been reported [18], [19]. However, in these schemes, only the concept has been introduced leaving ample scope for further investigation and insight into the design details.

The focus of this paper is to provide a detailed design procedure for selecting the external inductor which satisfies several practical constraints, allows DSTATCOM to regulate load voltage in stiff as well as resistive feeder, reduce the current requirement for mitigation of sag, and reduce the system losses. With coordinated control of the load fundamental current, terminal voltage, and voltage across the external inductor, a dynamic reference load voltage generation scheme is presented. This scheme ensures unity power factor (UPF) operation during normal operation and maintains load voltage constant during voltage disturbances. Detailed simulation and experimental results are included to verify the DSTATCOM performance.

OBJECTIVES
The objectives of this project is

- To provide a detailed design procedure for selecting the external inductor which satisfy several practical constraints, allows DSTATCOM to regulate load voltage in stiff as well as resistive feeder, reduce the current requirement for mitigation of sag, and reduce the system losses.
- With coordinated control of the load fundamental current, terminal voltage, and voltage across the external inductor, a dynamic reference load voltage generation scheme is presented.
- This scheme ensures unity power factor (UPF) operation during normal operation and maintains load voltage constant during voltage disturbances.
- Detailed simulation and experimental results are included to verify the DSTATCOM performance.

II. METHODOLOGY

2.1 DSTATCOM in Power Distribution System

Fig. shows power circuit diagram of the DSTATCOM topology connected in distribution system. *Ls* and *Rs* are source inductance and resistance, respectively. This inductor helps DSTATCOM to achieve load voltage regulation capability even in worst grid conditions, i.e., resistive or stiff grid. From IEEE-519 standard, point of common coupling (PCC) should be the point which is accessible to both the utility and the customer for direct measurement. The DSTATCOM is connected at the point where load and *Lext* are connected. The DSTATCOM uses a three-phase four-wire VSI.. Voltages across dc capacitors, *Vdc* 1 and *Vdc* 2, are maintained at a reference value of *Vdcref*.
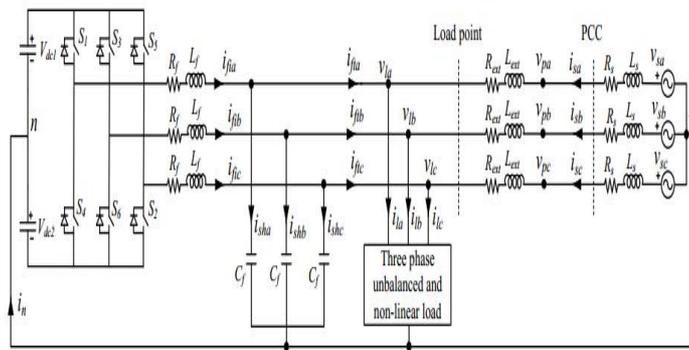
Fig.1 Phase equivalent circuit of DSTATCOM topology in distribution system

2.2 EFFECT OF FEEDER IMPEDANCE ON VOLTAGE REGULATION
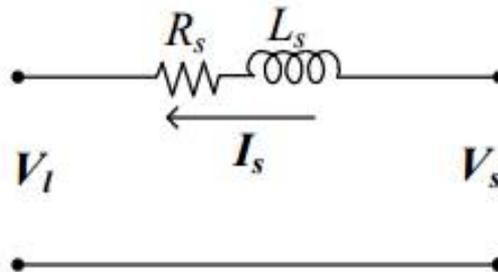
Fig.2 Equivalent source-load model without considering external inductor

To demonstrate the effect of feeder impedance on voltage regulation performance, an equivalent source-load model without considering external inductor is shown in Fig. 2. The current in the circuit is given as

$$I_s = \frac{V_s - V_l}{Z_s}$$

where $\mathbf{V}s = Vs \angle\delta$, $\mathbf{V}l = Vl \angle 0$, $\mathbf{I}s = Is \angle\varphi$, and $\mathbf{Z}s = Zs \angle\theta s$, with Vs, Vl, Is, Zs, δ, φ, and θs are rms source voltage, rms load voltage, rms source current, feeder impedance, load angle, power factor angle, and feeder impedance angle, respectively. The three phase average load power (Pl) is expressed as

$$P_l = Real[3V_l * I_s^*]$$

Substituting *Vl* and *Is* in , the load active power is

$$P_l = 3\frac{V_l^2}{Z_s}\left[\frac{V_s}{V_l}\cos(\theta_s - \delta)\right]$$

Rearranging above equation, expression for δ is computed as follows:

$$\delta = \theta_s - \cos^{-1}\left[\frac{V_l}{V_s}\cos\left(\theta_s + \frac{P_l Z_s}{3V_l^2}\right)\right]$$

For power transfer from source to load with stable operation in an inductive feeder, δ must be positive and less than 90◦. Also, all the terms of the second part of (4), i.e., inside cos− 1, are amplitude and will always be positiveThe vector expression for source voltage is given as follows:

$$V_s = V_l + I_s Z_s \angle (\theta_s + \emptyset)$$

A DSTATCOM regulates the load voltage by injecting fundamental reactive current. To demonstrate the DSTATCO voltage regulation capability at different supply voltages for different Rs/Xs, vector diagrams using (5) are drawn in Fig.3. To draw diagrams, load voltage Vl is taken as reference phasor having the nominal value OA (1.0 p.u.). With aim of making Vl = Vs = 1.0 p.u., locus of Vs will be a semicircle of radius Vl. Since, the maximum possible load angle is 90◦ in an inductive feeder, phasor Vs can be anywhere inside curve OACBO. Fig. considers case when Rs/Xs = √3 i.e., θs = 30◦. The area under ACDA shrinks, which shows that with the increase in Rs/Xs from the limiting value, the voltage regulation capability decreases. In this case the limiting values of Vslimit and IsZs are found to be 0.866 and 0.5 p.u., respectively. Here, maximum possible voltage regulation is 13.4%.
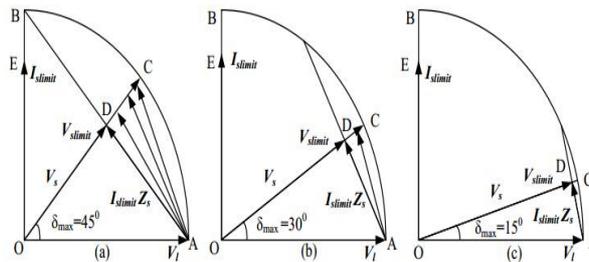
Fig.3 Regulation performance curve of DSTATCOM at different Rs /Xs. (a) For Rs /Xs = 1. (b) For Rs /Xs = √3. (c) For Rs /Xs = 3.73.

III. SELECTION OF EXTERNAL INDUCTOR FOR VOLTAGE

3.1 Regulation Improvement and Rating Reduction

This section presents a generalized procedure to select external inductor for improvement in DSTATCOM voltage regulation capability while reducing the current rating of VSI. Fig. 4 shows single phase equivalent DSTATCOM circuit diagram in distribution system. With balanced voltages, source current will be

$$I_s = \frac{Vs\angle\delta - V_l\angle 0}{(Rs + Rext) + j(Xs + Xext)}$$

$$I_s = \frac{Vs\angle\delta - V_l\angle 0}{(Rsef + jXsef)}$$

Where Rsef = Rs +Rext and Xsef = Xs +Xext are effective feeder resistance and reactance, respectively. Rext is equivalent series resistance (ESR) of external inductor, and will be small. With   and

$$\theta sef = \tan^{-1}\frac{Xsef}{Rsef}$$

$$Zsef = \sqrt{Xsef^2 + Rsef^2}$$

as effective impedance angle and effective feeder impedance, respectively, the imaginary component of Is is given as

$$I_s^{im} = \frac{V_l \sin\theta_{sef} + V_s \sin(\delta - \theta_{sef})}{Z_{sef}}$$

With the addition of external impedance, the effective feeder impedance becomes predominantly inductive. Hence, Zsef≈Xsef. Therefore, approximated Isim will be

$$I_s^{im} = \frac{V_l \sin\theta_{sef} + V_s \sin(\delta - \theta_{sef})}{X_{sef}}$$

DSTATCOM Power rating (Svsi) is given as follows:

$$S_{vsi} = \sqrt{3}\frac{V_{dc}}{\sqrt{2}} I_{vsi}$$

Where Ivsi is the rms phase current rating of the VSI and Vdc is the voltage maintained at the dc capacitors. The DSTATCOM aims to inject harmonic and reactive current component of load currents. Suppose Ilim is the maximum rms reactive and harmonic current rating of the load, then the value of
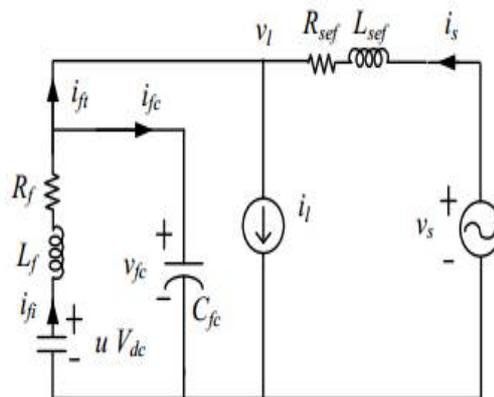
Fig.4 Single phase equivalent circuit of DSTATCOM topology with external inductor in distribution system.
Compensator current used for voltage regulation (same as Isim) is obtained by subtracting Ilim from Ivsi and given as follows:

$$I = I_{vsi} - I_l^{im} = \frac{\sqrt{2}S_{vsi}}{\sqrt{3}V_{dc}}$$

Comparing (8) and (10) while using value of δ from (4), following expression is obtained:

$$X_{sef} = \frac{V_l \sin\theta_{sef} + V_s \sin\left(\cos^{-1}\left[\frac{V_l}{V_s}\cos\left(\theta_{sef} + \frac{P_l X_{sef}}{3V_l^2}\right)\right]\right)}{\frac{\sqrt{2}S_{vsi}}{\sqrt{3}V_{dc}} - I_l^{im}}$$

The above expression is used to compute the value of external inductor. Design example of external inductor, used for this work, is given in next section.

IV. FLEXIBLE CONTROL STRATEGY

This section presents a flexible control strategy to improve the performance of DSTATCOM in presence of the external inductor Lext. Firstly, a dynamic reference load voltage based on the coordinated control of the load fundamental current, PCC voltage, and voltage across the external inductor is computed. Then, a proportional integral (PI) controller

is used to control the load angle which helps in regulating the dc bus voltage at a reference value. Finally, three phase reference load voltages are generated.

4.1. Derivation of Dynamic Reference Voltage Magnitude (VI*)

In conventional VCM operation of DSTATCOM, the reference load voltage is maintained at a constant value of 1.0 p.u. [10]–[12]. Source currents cannot be controlled in this reference generation scheme. Therefore, power factor will not be unity and source exchanges reactive power with the system even at nominal supply. To overcome this limitation, a flexible control strategy is developed to generate reference

SIMULATION PARAMETERS

System quantities	Values
Source voltage	230 V rms L-N (1.0 p.u.), 50 Hz
Feeder impedance	R_s = 0.3 Ω, L_s = 0.3 mH, R_s/X_s = 3.185
External impedance	L_{ext} = 6.7 mH, R_{ext} = 0.07 Ω
Linear load	Z_{la} = 30 + j62.8 Ω, Z_{lb} = 40 + j78.5 Ω, Z_{lc} = 50 + j50.24 Ω
Nonlinear load	Three phase rectifier supplying R-L load of 50 Ω and 200 mH
VSI parameters	V_{dc} = 520 V, C_{dc} = 2600 μF, L_f = 5 mH, C_f = 20 μF, S_{vsi} = 30 kVA
PI gains	$K_{p\delta}$ = 8.5e^{-7}, $K_{i\delta}$ = 1.8e^{-6}

1) Normal Operation:

It is defined as the condition when load voltage lies between 0.9 to 1.1 p.u. In this case, the proposed flexible control strategy controls load voltages such that the source currents are balanced sinusoidal and VSI does not exchange any reactive power with the source. Hence, the source supplies only fundamental positive sequence current component to support the average loads power and VSI losses.

$$I_{sj}^* = \frac{V_{pj1}^+}{\Delta_1^+}(P_l + P_{loss})$$

$$P_l = \frac{1}{T}\int_{t1-T}^{t1}(v_{1a}i_{1a} + v_{1b}i_{1b} + v_{1c}i_{1c})dt$$

$$P_{loss} = \frac{1}{T}\int_{t1-T}^{t1}(v_{1a}i_{1ta} + v_{1b}i_{1tb} + v_{1c}i_{1tc})dt$$

The reference source currents must be in phase with the respective phase fundamental positive sequence PCC voltages for achieving UPF at the PCC. Instantaneous PCC voltage and reference source current in phase-a can be defined as follows:

$$V_{pa1}^+ = \sqrt{2}V_{pa1}^+\sin(\omega t - \varphi_{pa1}^+)$$
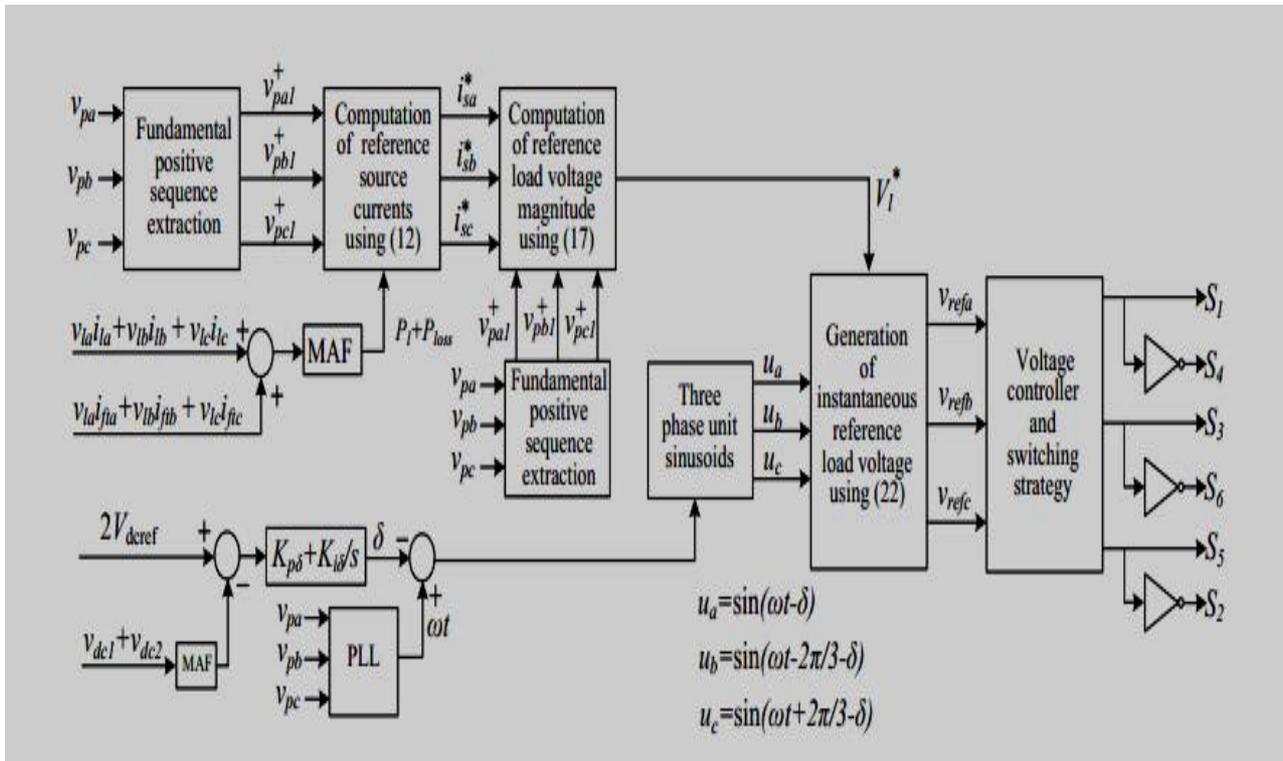
Fig.5 Block diagram of proposed flexible control strategy

$$I_{sa}^* = \sqrt{2}I_{sa}^* \sin(\omega t - \varphi_{pa1}^+)$$

Where V+pa1 and ϕ+pa1 are rms voltage and angle of fundamental positive sequence voltage in phase-a, respectively.

$$V_{ta} = V_{pa1}^+ - I_{sa}^* Z_{sext}$$

V. SIMULATION RESULTS

The parameters of DSTATCOM compensated distribution system are given in Table I. Usual scenario in distribution system having resistive feeder impedance are considered. PSCAD software is used to simulate the system. Firstly, the DSTATCOM is operated in conventional VCM, i.e.

1) Without external inductor and 2) with a reference voltage of 1.0 p.u. or 230 V rms. The steady state waveforms of three phase PCC voltages, load voltages, source currents, filter currents, and load currents are shown in Figs. 7(a)-(e), respectively.

Here, the DSTATCOM has to compensate only for feeder drop. However, from the load voltage waveform shown in Fig. 7(b), its magnitude is found to be 227.7 V. This large reactive current is supplied by the VSI, as shown in Fig. 7(d), which increases its current rating. The load voltages and source currents waveforms are shown in Figs. 8(ii) and (iii), respectively. These waveforms are balanced and sinusoidal. Also, UPF is achieved at the PCC. Hence, compensator supplies only load harmonic and reactive.

EXPERIMENTAL SETUP PARAMETERS

System quantities	Values
Source voltage	50 V rms L-N (1.0 p.u.), 50 Hz
Feeder impedance	$R_s = 0.3\ \Omega$, $L_s = 0.3$ mH, $R_s/X_s = 3.185$
External impedance	$L_{ext} = 6.7$ mH, $R_{ext} = 0.07\ \Omega$
Linear load	$Z_{l_a} = 30 + j31.4\ \Omega$, $Z_{l_b} = 40 + j16\ \Omega$, $Z_{l_c} = 50 + j31.4\ \Omega$
Nonlinear load	Three phase rectifier supplying R-L load of 50 Ω and 100 mH
VSI parameters	$V_{dc} = 130$ V, $C_{dc} = 2600\ \mu F$, $L_f = 5$ mH, $C_f = 20\ \mu F$
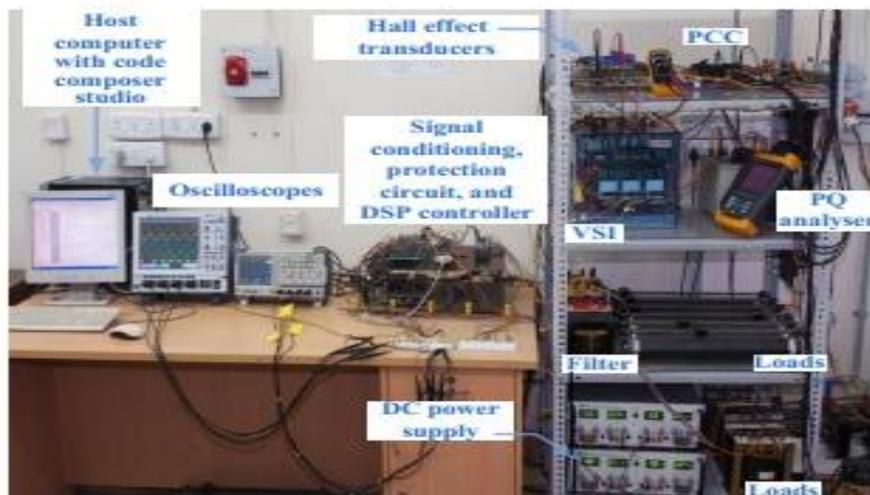
Fig.6 Photograph of experimental setup

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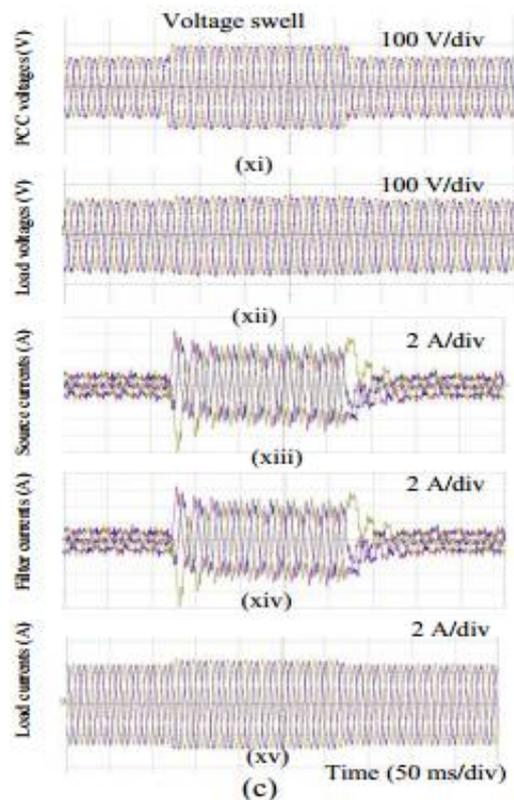
Fig.7 Experimental results. (a) During normal operation (i)-(v). (b) During voltage sag (vi)-(x). (c) During voltage swell (xi)-(xv).

Power in addition to reactive power requirement of the Lext. The THDs in the load currents are 14.5%, 15.3%, and 13.6% for phases a, b, and c, respectively. After the compensation, the THDs in source currents are reduced to 2.4%, 2.7%, and 2.4%, respectively in phases a, b, and c. The filter and load currents are shown in Figs. 8(iv) and (v), respectively. These waveforms validate the performance of flexible control strategy as

1) source does not exchange reactive power from the system,
2) filter does not supply additional current and reduces system losses, and
3) UPF is maintained at the PCC.

These features are not available in conventional DSTATCOM operating in VCM.

Approximate losses in the system are given as follows:

$$P_{loss} = 3\left(I_{f1}^2 R_f + (I_s^{im})^2 R_s + (I_s^{real})^2 R_s\right)$$

In conventional scheme, the source always exchanges reactive power. Hence, Isim will be non-zero. Also, this current is supplied by the filter i.e., If1 will be higher. However, in proposed scheme, it is seen that the source does not exchange reactive power in normal operation. Hence, Isim = 0 and If1 is reduced. Hence, proposed scheme reduces losses in the system and utilizes smaller VSI ratings. Small power losses will be there due to the ESR of the external inductor. However, the losses in the ESR will be much smaller than that of reduction of power losses from the conventional DSTATCOM operation. Voltage sag is created by reducing the source voltage to 0.6 p.u. at t = 0.3 s for 4 cycles. Fig. 8(vi) shows the PCC voltages. Control of reference load voltage based on the coordinated control of fundamental load current, PCC voltage, and voltage across the external inductor allows DSTATCOM to set different constant reference voltage. The proposed scheme detects voltage sag and load voltage is changed to 0.9 p.u.

The waveforms of load voltages are shown in Fig. 8(vii).

This guarantees continuous, flexible, and robust operation of the load. The source currents are increased during sag period as illustrated in Fig. 8(viii). Fig. 8(ix) shows the filter currents which increase during sag period to support the load voltage. The load currents waveforms presented in Fig. 8(x) is nearly constant during entire operation. Once the sag is removed at t = 0.38 s, slowly all the waveforms reach the pre-sag values. With the results of Figs. 8(vi)-(x), it can be concluded that the proposed scheme makes load operation continuous.

Source voltage is increased to 1.4 p.u. at t = 0.8 s to create swell. The PCC voltages are shown in Fig. 8(xi). The algorithm detects swell and maintains load voltage at 1.1 p.u. The waveforms are shown in Fig. 8(xii). The waveforms of the source, filter, and load currents are shown in Figs. 8(xiii)- (xv), respectively. The filter currents increase during swell which increases the source currents as well. Load currents are nearly constant throughout the operation. Once sag is removed, it is detected by the algorithm and system is brought to the steady state conditions. It confirms effectiveness of the proposed scheme.

VI. EXPERIMENTAL RESULTS

A reduced scale experimental prototype, as shown in Fig., is developed to validate the capability of proposed scheme. The parameters of the system are given in Table II. Performance of the DSTATCOM and flexible control strategy at the steady state is shown in Fig. 10(a). The three phase PCC voltages, load voltages, source currents, filter currents, and load currents are shown in Figs. 10(i)-(v), respectively.

The scheme makes both three phase source currents as well as load voltages balanced and sinusoidal. The THDs in the load currents are 18.1%, 17.5%, and 19.4% for phases a, b, and c, respectively. After the compensation, the THDs in source currents are reduced to 3.2%, 3.6%, and 3.4%, in respective phases. Also, source currents are in-phase with the respective PCC voltages. It confirms that the source does not exchange any reactive power with the system. Therefore, the filter currents consist of harmonic and reactive component of load current in addition to reactive current requirement of external inductor. The performance of the proposed scheme during voltage sag is shown in Fig. 10. The PCC voltages shown in Fig. are decreased to 0.6 p.u. during the sag period. The control strategy detects sag and maintains load voltage, as shown in Fig. 10(vii), at 0.9 p.u. during the entire sag period. Moreover, no transient in the load voltage is noticed. It can be observed from Fig. That the source currents are increased during the sag duration. It is due to the fact that the compensator supplies reactive current, as shown in Fig, towards the source to maintain load voltage at a constant value. The load currents are shown in Fig. 10(x). These are drawn as per the load requirement.

VII. CONCLUSION

This paper has presented design, operation, and control of a DSTATCOM operating in voltage control mode (VCM). After providing a detailed exploration of voltage regulation capability of DSTATCOM under various feeder scenarios, a benchmark design procedure for selecting suitable value of external inductor is proposed. An algorithm is formulated for dynamic reference load voltage magnitude generation. The DSTATCOM has improved voltage regulation capability with a reduced current rating VSI, reduced losses in the VSI and feeder. Also, dynamic reference load voltage generation scheme allows DSTATCOM to set different constant reference voltage during voltage disturbances. Simulation and experimental results validate the effectiveness of the proposed solution. The external inductor is a very simple and cheap solution for improving the voltage regulation, however it remains connected throughout the operation and continuous voltage drop across it occurs. The future work includes operation of this fixed inductor as a controlled reactor so that its effect can be minimized by varying its inductance.

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